A computation-universal two-dimensional 8-state triangular reversible cellular automaton

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Abstract

A reversible cellular automaton (RCA) is a cellular automaton (CA) whose global function is injective and every configuration has at most one predecessor. Margolus showed that there is a computation-universal two-dimensional 2-state RCA. But his RCA has non-uniform neighbor, so Morita and Ueno proposed 16-state computation-universal RCA using partitioned cellular automata (PCA). Because PCA can be regarded as a subclass of standard CA, their models has standard neighbor. In this paper, we show that the number of states of Morita and Ueno's models can be reducible. To decrease the number of states from their models with preserving isotropic and bit-preserving properties, we used triangular 3-neighbor, and thus 8-state RCA can be possible. This is the smallest state two-dimensional RCA under the condition of isotropic property on the framework of PCA. We show that our model can simulate basic circuit elements such as unit wires, delay elements, crossing wires, switch gates and inverse switch gates. And it is possible to construct a Fredkin gate by combining these elements. Since Fredkin gate is known to be a universal logic gate, our model has computation-universality.

Keywords: cellular automata, reversibility, computation-universality, conservative logic.

1 Introduction

A reversible cellular automaton (RCA) is a cellular automaton (CA) whose global function is injective and every configuration has at most one predecessor. Reversibility is a very strong constraint, but computation-universality of RCA has been showed [2].

On two-dimensional CA, their computation-universality can be proved by embedding universal logic elements. For example, computation-universality of the game of life was proved by constructing AND, OR, NOT, and fan-out gates on its cellular space. Sequences of glider patterns was used as signal carriers [1]. Using this approach, one can construct small state computation-universal CA. But on RCA, erasing informations are inhibited and such irreversible logic gates can not be embedded directly. Margolus proposed a two-dimensional computation-universal RCA (BBMCA) [4]. He realized its universality by embedding Fredkin and Toffoli's Billiard Ball Model (BBM). BBM is a computing model in which logical operations are performed by elastic collisions of balls. They showed that 3-input, 3-output reversible and bit-preserving Fredkin gate (F-gate) can be embedded in their BBM, and combining F-gates and unit delays, any logic circuits can be constructed using BBM.

Although BBMCA is simple RCA, it has non-uniform neighbor. So Morita and Ueno proposed a different type of 4-neighbor 16-state computation-universal RCA [5]. They used a partitioned cellular automaton (PCA). It is regarded as a subclass of standard CA. In PCA, the injectivity of a global function is equivalent to the injectivity of local function and it makes ease of constructing RCA [6].

In this paper, we show that the number of states of Morita and Ueno's models can be reduced. To decrease the number of states from their models with preserving isotropic and bit-preserving properties, we used triangular 3-neighbor, and thus 8-state RCA can be possible. This is the smallest state two-dimensional RCA under the condition of isotropic property on the framework of PCA.

2 Computation-universal RCA and BBM

2.1 Fredkin Gate

On BBMCA and 16-state RPCA models, BBM is used for showing their computation-universality. First we make a brief description about BBM and a Fredkin gate.

A Fredkin gate (F-gate) is a basic element in the theory of Conservative Logic proposed by Fredkin and Toffoli [3]. It is reversible and bit-preserving logic gate (Fig. 1). They showed that AND, OR, NOT, and fan-out gate can be constructed by an F-gate and any circuits can be constructed by F-gates and unit delays.

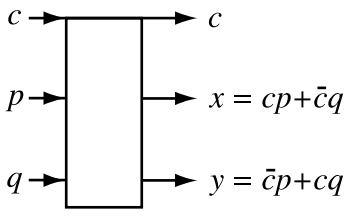

Figure 1: A Fredkin gate

They also introduced a switch gate (S-gate) and its inverse gate (Fig. 2). An S-gate is a 2-input, 3-output reversible and bit-preserving logic gate. An S-gate switches the input x by

the control signal c. They showed that S-gates can be constructed on their Billiard Ball Model (BBM) and using two S-gates and two inverse S-gates, it is possible to construct an F-gate (Fig. 3).

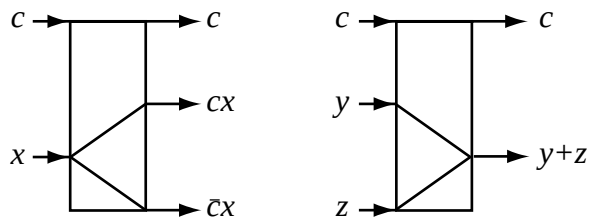

Figure 2: An S-gate and an inverse S-gate

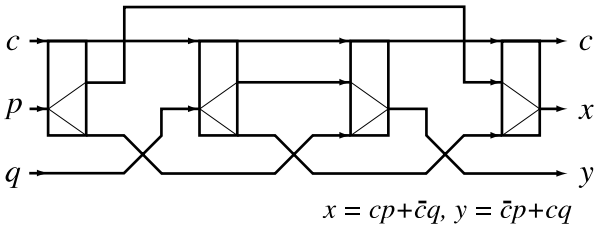

Figure 3: A realization of a Fredkin gate by S-gates and inverse S-gates

2.2 Computation-universal RPCA

Though BBMCA uses a non-uniform neighborhood, Morita and Ueno constructed 16-State two-dimensional computation-universal RCA using the framework of partitioned cellular automata (PCA) [5]. PCA is regarded as the subclass of standard CA. Each cell is partitioned into the equal number of parts to the neighborhood size and the information stored in each part is sent to only one of the neighboring cells. In PCA, injectivity of global function is equivalent to injectivity of local function, thus a PCA is reversible if its local function is injective [6]. Their models used 4-neighbor PCA and fig. 4 shows its domain and range of the local function.

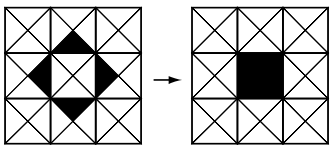

Figure 4: Domain and range of local function in 2D 4-neighbor PCA

They proposed two models and fig. 5 is the local function of one of their models.
Their RPCA has following properties.

(i) bit-preserving: the number of "1" cells (i.e. black cells) on both side of the transition rules is the same.

(ii) isotropic: the local function is invariant under the rotation of 90, 180, 270 degrees(90-degree isotropic).

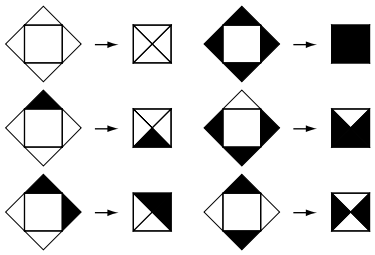

Figure 5: The local function of 2D 16-state 4-neighbor RPCA

They proved its computation-universality by constructing S-gates, Inverse S-gates and F-gates on its cellular space.

3 Two-dimensional triangular RPCA

3.1 8-state triangular RPCA

To decrease the number of states from Morita and Ueno's model with preserving bit-preserving and isotropic properties, we used triangular 3-neighbor, and thus 8-state PCA can be possible. Fig. 6 shows domain and range of a local function. This is the smallest state two-dimensional PCA under the condition of isotropic property.

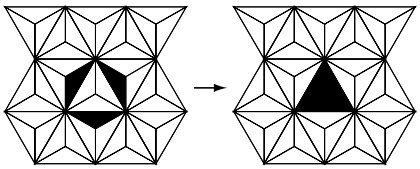

Figure 6: Domain and range of local function in 3-neighbor triangular PCA

There are nine bit-conserving and 120-degree isotropic local function by combining four rules out of eight rules depicted in fig. 7 . And there are five different local functions excluding symmetric cases.

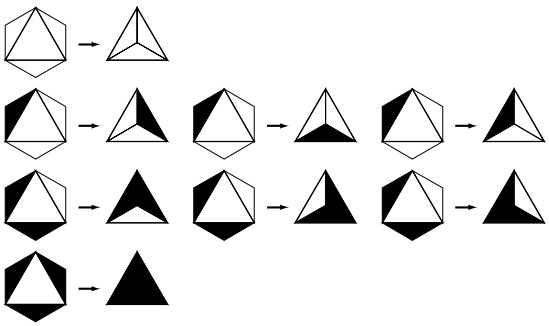

Figure 7: Isotropic transition rules in 3-neighbor triangular PCA

3.2 A computation-universal 8-state model

We show that the RPCA which local function is given by fig. 8 is computation universal.

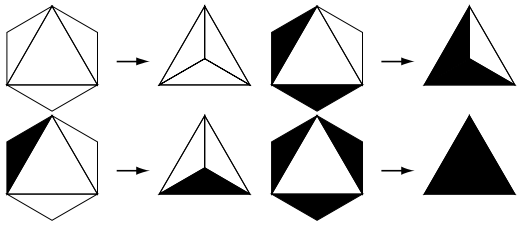

Figure 8: The local function of 3-neighbor triangular RPCA

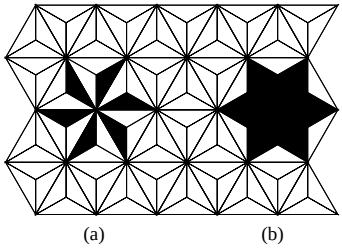

Figure 9: Stable blocks

First, we construct signal transmission wires.

On the proof of computation-universality of the game of life, gliders were used to encode signals [1]. In the same way, BBMCA [4] and 16-state RPCA models [5] used "ball"s. They propagate on a quiescent cellular space as signal carriers. Although on this model, it is difficult to construct simple patterns propagating on a quiescent cellular space, there are two simple stable blocks shown in fig. 9 , and combining (b)-type blocks, it is possible to construct signal transmission wires (Fig. 10). A block as a signal carrier is shown in gray color. The gray block

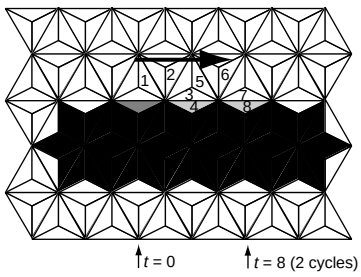

Figure 10: A data transmission wire

takes 4 steps (regarded as 1 cycle) to move to the next dent (the part shown as the number 4).

A 4 steps (1 cycle) delay element is shown in fig. 11 (a) This wire has a cave and signals take 4 steps in travelling through it. This delay element can be used as synchronization element for changing columns/rows of transmission wires.

The transmission wire depicted in fig. 11 (b) changes its row by two lines. The wire contains one right turning and one left turning, so signals are propagating on the wire with strictly 4 step (1 cycle) delays. Then if the straight wire contains a delay element (Fig. 11 (a)), both signals can be synchronized.

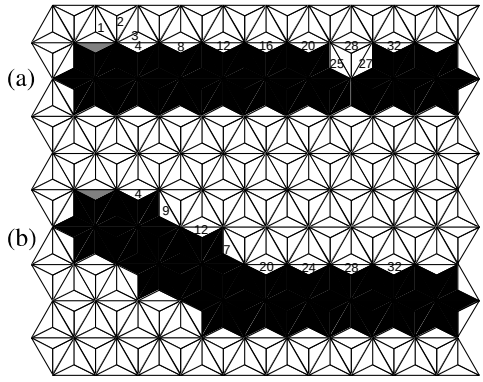

Figure 11: A delay element

When a circuit contains feedback loop like fig. 12 , the transmission wire turns right/left six times, and thus output signal phase of the feedback wire differs from that of input signal by ± 2 steps(± 0.5 cycles). But delay element of ± 2 steps can be constructed by the crossing of two

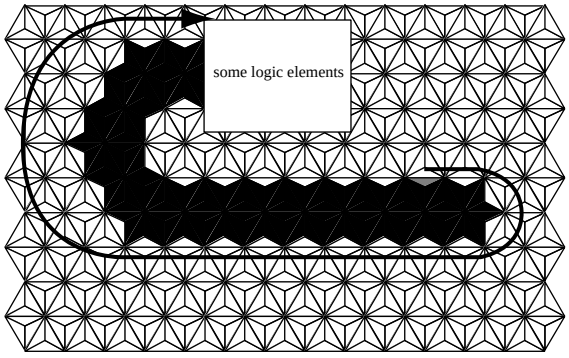

Figure 12: A feedback wire

signals. Fig. 13(a) is a -2 steps phase shifter. The stable star shaped block above the horizonal wire has a "fin", and it turns around the 6 branches of the block in 30 steps. When this fin crosses the arriving signal along the wire, it advances the phase of the signal 2 steps. So this -2 steps phase shifter accepts signals every 30 steps. And combining a delay element, $+2$ steps shifter can be also available (Fig. 13(b)).

This model uses connected stable blocks for transmission wires and we need special structure to realize crossing wires. Fig. 14 shows a module for crossing wires. Rotating "fin"s switch signals from two input wires to each output wires. This crossing element accepts signals every 30 steps

We showed that it can be possible to realize signal transmission wires, delay elements, phase shifters and crossing wires. Next we show the function of S-gates and inverse S-gates can be available.

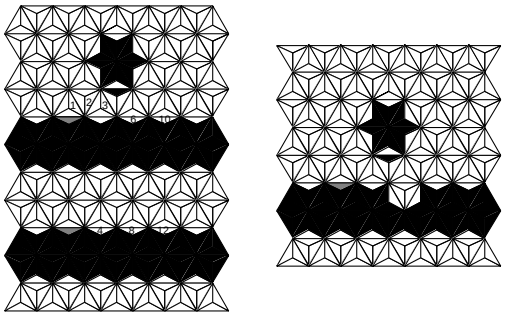

Figure 13: Phase shifters (a) -2, (b) $+2$

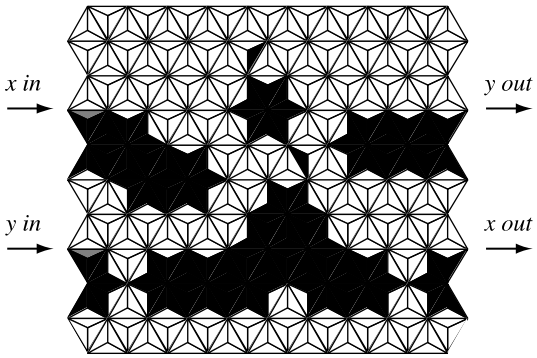

Figure 14: A crossing element

A cell can be regarded as a 3-input, 3-output gate. Although an F-gate is also a 3-input, 3-output gate, it cannot be possible to realize under the isotropic condition. But S-gate and inverse S-gate can be constructed by isotropic condition. Fig. 15 shows the input/output relations of an S-gate and an inverse S-gate.

Fig. 16 shows an S-gate with synchronizing phase shifters. This element takes 40 steps (10 cycles) to generate output signals and input must be given every 30 steps. Although all input/output signals in fig. 16 are synchronized, it does not fit the definition of the S-gate in fig. 2. Because the output terminal of signal "c" is placed in the opposite side of this element. Then we show a complete pattern of an S-gate in fig. 17. In this pattern, an output signal "c" travells along a feedback wire and a crossing element, and it has a long delay against other output signals. so the right part of this patters are used to synchronize all output signals. This element takes 140 steps to generate output signals and inputs must be given every 30 steps.

Because an S-gate and an inverse S-gate are symmetric, an inverse S-gate can be constructed by reflecting a pattern of this S-gate with simple modifications of rotating "fin"s. It is shown in fig. 18.

Combining circuit elements mentioned above, an F-gate is constructed by fig. 3 (fig. 19). It takes 704 steps (176 cycles) to simulate an F-gate.

4 Conclusion

In this paper, we have constructed an 8-state triangular RPCA which has computation universality. It is the smallest state RPCA with bit-preserving and isotropic local functions. It is an

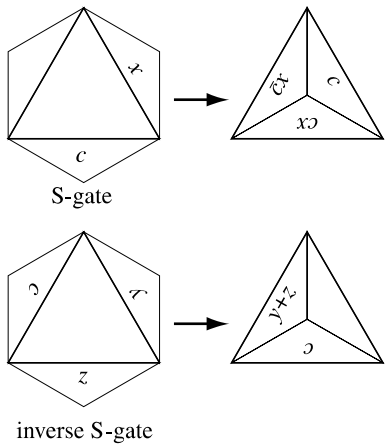

Figure 15: Construction of S-gate and inverse S-gate

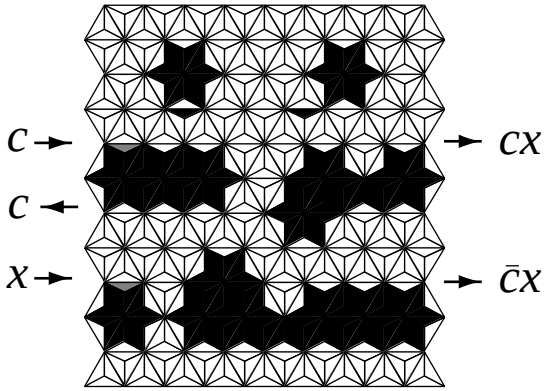

Figure 16: An S-gate with phase shifter

open problem to find other 8-state universal RPCA.

References

[1] Berlekamp, E., Conway, J., Guy, R.: *Winning Ways for Your Mathematical Plays*, **Vol. 2**, Academic Press, New York (1982).

[2] Toffoli, T.: Computation and construction universality of reversible cellular automata, *J. Comput. Syst. Sci.*, **15** (1977) 213–231.

[3] Fredkin, E., Toffoli, T.: Conservative logic, *Int. J. Theoretical Physics*, **21**, 3/4 (1982) 219–253.

[4] Margolus, N.: Physics-like models of computation, *Physica*, **D10** (1984) 81–95.

[5] Morita, K., Ueno, S: Computation-universal models of two-dimensional 16-state reversible cellular automata, *IEICE Trans. Inf. & Syst.*, **E75-D** (1992) 141–147.

[6] Morita, K.,Harao, M.: Computation universality of one-dimensional reversible (injective) cellular automata, *Trans. IEICE*, **E72** (1989) 758–762.

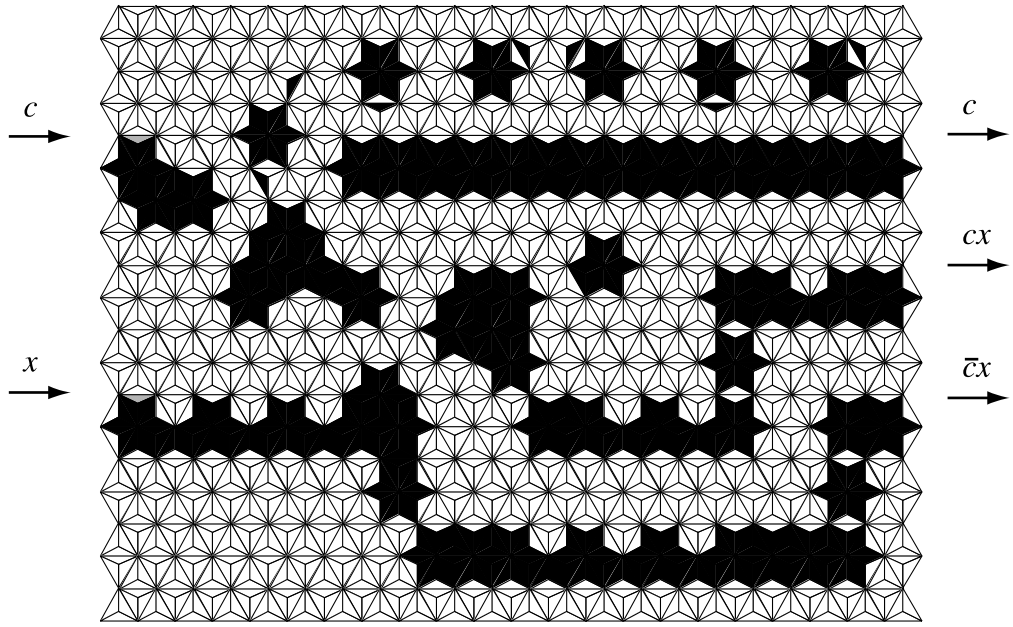

Figure 17: A configuration of S-gate

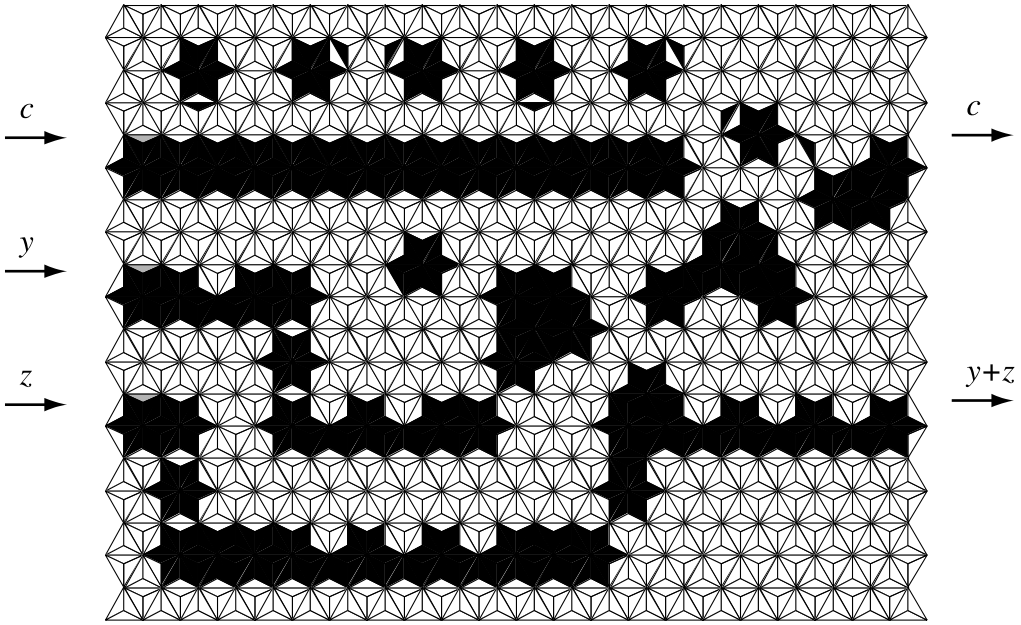

Figure 18: A configuration of inverse S-gate

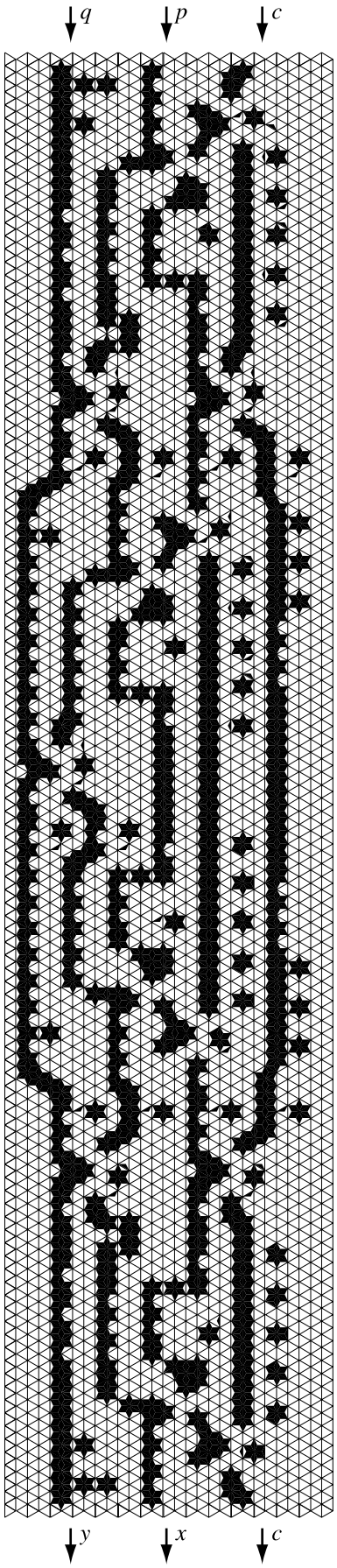

Figure 19: A configuration of F-gate